

Course Syllabus: EET-141 Digital Circuits Spring 2007

Lecture Instructor: _____

Office: _____ Phone # _____ ext. _____

Lab Instructor: _____

Office - _____ Phone # _____ ext. _____

COURSE DESCRIPTION:

This course is an introduction to the theory and design of logic circuits used in computers and other digital equipment. Topics covered include introduction to digital systems, binary numbers, binary logic gates, combinational logic and simplification techniques, data selector logic, encoders and decoders, flip-flops, counters, shift registers, binary arithmetic, memories and analog-to-digital and digital-to-analog conversion.

I. Class Meetings

3 hours per week class time allocated for Lecture / HW

3 hours per week class time allocated for Lab

II. Course MaterialsA. Text: Digital Fundamentals, 9th Edition, by Thomas L. Floyd, Prentice Hall, 2006

B. Course Objectives, Lectures and Homework: Provided

C. Laboratory Manual / Material: Provided

D. Laboratory Logbook: "5-squares to the inch"

Must be similar to the Roaring Springs "Compositions" notebook,
9 $\frac{3}{4}$ x 7 $\frac{1}{2}$, 100 leaves. [Lab Instructor will provide at cost]

III. Evaluation

A. Two (2) excused absences are permitted per term. Call the instructor to be excused. If a student's absences are excessive, the instructor may drop that student from the course.

B. Calculation of Final Grade Point Average:

- Chapter Homework (Instructor will review for completeness) 10%
 - To be done in a bound or spiral notebook. - Due on the day of Chapter Test
 - Late policy: Instructor will accept no more than one homework per week.

Ex: If you turn in five (5) home works to be graded during the last week, four will receive a zero (0).
- Tests 60%
 - Tests are typically given in class. To be excused from a test you must phone or email the instructor *before* the test is to be taken. (Your instructor will indicate his/her preferred method of contact.)
 - *You will be given the opportunity to make up excused tests during an assigned make-period **during the final examination week**.* This make-up test will be similar to the excused test. The time and date of this make up test will be assigned after the "Official

Chapter #1 Introductory Digital Concepts

Objectives:

- Explain the difference between analog and digital quantities
- Show how voltage levels are used to represent digital quantities
- Describe various parameters of a pulse
- Explain the basic logic operations of NOT, AND and OR waveform
- Describe the logic functions of the comparator, adder and other logic circuits
- Identify fixed function digital integrated circuits according to their complexity and the type of circuit packaging
- Describe the programmable logic device (PLD) and discuss how they are programmed
- Recognize and understand digital test instruments
- Show how a complete digital system is formed from the basic functions for a "Tablet-Counting and Bottling Control System"

Reading:

- Read Chapter 1 Introductory Digital Concepts
- Read "Digital System Application (P. 38)"

System Assignment:

- None

Homework: (Answers to odd numbered problems are at the back of your text) [even answers]

- 3, 5
- 6 [4 ms], 7, 8 [periodic, it repeats at a fixed interval], 9
- 10 [10101110]
- 12 [AND], 13, 14 [OR]
- 15, 16 [1000]
- 20
- 21, 23
- 28, 29

Laboratory:

1. Introduction to the Laboratory Logbook Method and Measurement of Nonlinear Pulse Characteristics

Chapter #2 Numbering Systems, Operations and Codes

Objectives:

- Review decimal numbering systems
- Count in the binary numbering system
- Convert from decimal to binary and from binary to decimal
- Apply arithmetic operations to binary systems
- Determine the 1's and 2's complements of a binary number
- Express signed binary numbers in 2's complement format (We will only use 2's complement form)
- Perform addition with 2's complement signed binary numbers
- Convert between the binary and hexadecimal numbering system and add numbers in hexadecimal form
- Express decimal numbers in binary coded decimal (BCD) form
- Demonstrated binary codes including the American Standard Code for Information Interchange (ASCII)
- Use binary numbers and codes in "Tablet Counting and Bottling Control System"

Reading:

- Read Chapter #2 Numbering Systems, Operations and Codes *with the following exceptions:*
 - Sec. 2-6 Signed Numbers, Skip Floating-Point Numbers, P. 65-67
 - Sec. 2-7 Arithmetic Operations, Skip Multiplication and Division, P. 70 (bottom) – 74

Homework: (Answers to odd numbered problems are at the back of your text) [even answers]

1

7a, 7b, 7c, 8 [3, 7, 15, 31, 63, 127, 255, 511, 1023, 2047]

11a, 11b, 11c, 13e, 13f, 13g, 13h

15d, 15e, 15f, 17a, 17b, 17c

19d, 19e, 19f, 20g [01010000], 20h [11000011]

23b, 23c, 23d, 26a [-103], 26b [+116], 26c [-65]

29a, 29b, 29c, 29d

35a, 35b, 36(a-f) [E, 2, 17, A6, 3F0, 982], 37a, 37b, 39a, 39b, 40a [11]. 40b [8E]

45a, 45b, 45c, 48d [18], 48e [19], 48f [32]

57a, 57b, 57c, 60 (use HEX) [33, 30, 20, 49, 4E, 50, 55, 54, 20, 41, 2C, 42], 61a, 61b, 61c

System Assignment: None

Laboratory: 2. Building and Testing an Astable Multivibrator

Chapter #3 Logic Gates

Objectives:

- Describe the operation of the NOT, the AND and the OR gate
- Describe the operation of the NAND gate and the NOR gate
- Express the operation of the NOT, AND, OR, NAND and NOR gates with Boolean algebra
- Describe the operation of the exclusive-OR and exclusive NOR gates
- Recognize and use the distinctive shape logic symbols
- Construct timing diagrams showing the proper time relations of inputs and outputs for various logic gates
- Make basic comparisons between the major IC technologies – CMOS and TTL
- Define propagation delay, power dissipation, speed-power product, and fan-out in relation to logic gates
- Use each logic gate in simple applications
- Troubleshoot logic gates
- Describe the basic concepts of programmable logic

Reading:

Read Chapter #3 Logic Gates

Homework: (Answers to odd numbered problems are at the back of your text) [even answers]

2

3, 5

7, 8 [X goes low 4 times when A, B, C are all low: At the start, twice in the middle and at the end]

11, 14 [Refer to the truth table on P 3-7 of your lecture, two ways to derive the output waveform (1) the output wave is low when *both* inputs are high or (2) the output is high if *either* input is low]

18 [Refer to the truth table on P 3-9 of your lecture, two ways to derive the output waveform (1) the output wave is low if *either* input is high or (2) the output is high if *both* inputs is low]

19

23, 24

25, 26 [(a) 16.5mW, (b) 2.7V, (c) 15ns, (d) 0.4V (max), (e) at 2V, 75ns, 75ns, at 6V, 13ns, 13ns],

29

31

32 [(a) NAND gate faulty. Input A open (b) NOR gate faulty. Input B shorted to ground (c) NAND gate ok (d) XOR gate faulty. Input open],

34 [Timer input to AND gate open. Check for 30sec. HIGH level on this input when ignition is turned on]

35

Laboratory:

3. Introduction to Logic Gates

4. TTL Characteristics

Chapter #4 Boolean Algebra and Logic Simplification (Selected readings)

Objectives:

- Apply the basic laws and rules of Boolean algebra
- Apply DeMorgan's theorems to Boolean expressions
- Describe gate networks with Boolean expressions
- Convert any Boolean expression a sum-of-products (SOP)
- Use a Karnaugh map to simplify Boolean expressions
- Apply Boolean algebra and the Karnaugh map methods to a system application

Read Chapter #4 Boolean Algebra and Logic Simplification with the following modifications:

Sec 4.1 Boolean Operations and Expressions: *Read all*

Sec. 4-2 Laws and Rules of Boolean Algebra: *Read all*

Sec. 4.3: Demorgan's theorems: Read P. 191-192 (through Ex. 4-3 ONLY)

Sec. 4-4: Boolean Analysis of Logic Circuits: *Read all*

Sec. 4-5: Simplification Using Boolean Algebra: SKIP

Sec. 4-6: Standard Forms of Boolean Expressions: Read P 200 "The Sum-of-Products (SOP) Form" sub-section and P. 203 "The Product-of-Sums (POS) Form" sub-section ONLY

Sec. 4-7 Boolean Expressions and Truth Tables: *Read all*

Sec 4-8 The Karnaugh Map: *Read all*

Sec 4-9 Karnaugh Map SOP Minimization: *Read all*

Sec 4-10 Karnaugh Map POS Minimization: SKIP

Sec. 4-11 Five-Variable Karnaugh Maps: SKIP

Sec. 4-12 VHDS: SKIP

P. 230 - 233 Digital System Application: *Read all*

Homework Problems: (Answers to odd numbered problems are at the back of your text) [selected even answers]

1, 3, 4 [1, 1, 0, 1, 0, 1]

7

9a, 9b

12, 13, 15a, 15b, 15c

21a, 21b

29a, 29b

34a, use SOP only [$x=(a+b+c)(a+B+c)(A+B+c)$]

34b, use SOP only [$x=(a+b+c)(a+b+C)(a+B+c)(a+B+C)(A+b+c)$]

35, 37

38a [AB+Bc], 38b [ac], 38c [B], 38d [C]

39, 43

System Assignment (P. 233): Activity 1 and 2 only

Laboratory: 5 Combinational Logic Circuits using NAND/NOT Logic

Chapter #5 Combinational Logic (Selected readings)

Objectives:

- Analyze basic combinational logic circuits, such as AND-OR and exclusive-OR
- Use AND-OR and AND-OR-Invert to implement sum-of-products (SOP) and product-of-sum (POS) expressions
- Design a combinational logic circuit for a given Boolean output expression
- Design a combinational logic circuit for a given truth table
- Use NAND gates to implement any combinational logic function
- Troubleshoot logic circuits by using signal tracing and waveforms
- Apply combinational logic to a system application

Read Chapter #5 Combinational Logic with the following modifications:

- Sec. 5-1 Basic Combinational Logic Circuits: *Read all*
- Sec. 5-2 Implementing Combinational Logic: *Read all*
- Sec. 5-3 The Universal Property of NAND and NOR Gates: *Read all*
- Sec. 5-4 Combinational Logic using NAND and NOR Gates: *Read all but do not worry about the algebra method of conversion. (The “double bubble” method will be examined in lecture.)*
- Sec. 5-5: Logic Circuit Operation with Pulse waveforms: *Read all*
- Sec. 5-6 Troubleshooting: *Read all*
- Sec. 5-7: Programmable Logic: *Read all*
- P. 278-281 Digital System Application: *Read all*

Homework Problems: (Answers to odd numbered problems are at the back of your text) [selected even answers]

3a, 3b, 3c, 3d, 5a, 5b, 5c, 5d

9a, 9b, 9c, 9d, 11 (use the Karnaugh map method to simplify)

42 [$X = \overline{AB} + \overline{CD} = ABCD$]

39

System Assignment (P. 281) activity 1 and 2 only

Laboratory: 5 Combinational Logic Circuits using NAND/NOT Logic (cont)

Chapter #6 Functions of Combinational Logic (Selected readings)

Objectives:

- Distinguish between half-adders and full-adders
- Use the magnitude comparator to determine the relationship between two binary numbers
- Implement a basic binary decoder
- Use BCD-to-7-segment decoders in display systems
- Apply multiplexers in data selection, multiplexed displays and simple communications systems
- Use decoders as demultiplexers
- Identify glitches, common bugs in digital systems
- Describe basically how SPLDs are programmed

Read Chapter #6 Functions of Combinational Logic with the following modifications:

- Sec. 6-1 Basic Adders: *Read all*
- Sec. 6-2 Parallel Binary Adders: Skip
- Sec. 6-3 Ripple Carry vs. Look-Ahead: SKIP
- Sec. 6-4 Comparators: *Read all*
- Sec. 6-5 Decoders: *Read all*
- Sec. 6-6 Encoders: *Read all*
- Sec. 6-7 Code Converters: Skip
- Sec. 6-8 Multiplexers: *Read all*
- Sec. 6-9 Demultiplexers: *Read all*
- Sec. 6-10 Parity Generators / Checkers: Skip
- Sec. 6-11 Troubleshooting: *Read all*
- P. 348 - 352 Digital System Application: Give it a try, for your information only

Homework Problems: (Answers to odd numbered problems are at the back of your text)
[selected even answers]

1a, 1b, 2a [$A = 0, B = 0, C_{in} = 0$], 2b [100 or 010 or 001]

11, 12

14a [$A_3A_2A_1A_0 = 1110$], 14b [1100], 14c [1111], 14d [1000], 15a, 15b, 15c, 18 [HLHHL]

22 [Hint: Which pin has highest priority?]

26 [D_1 is selected], 27

33a, 33b, 33c

Laboratory 6: BCD to 7-Segment Decoder / Driver and Data Selector / Multiplexer

Chapter #7 Flip-Flops and Related Devices

Objectives:

- Use logic gates to construct basic latches
- Explain the difference between an S-R latch and a D latch
- Explain how S-R, D and J-K flip-flops differ
- Understand the significance of propagation delays, set-up time, hold time, maximum operating frequency, minimum clock-pulse widths, and power dissipation in the application of flip-flops
- Explain how a one-shot operate
- Connect a 555 timer to operate as either an astable multivibrator or a one-shot
- Troubleshoot basic flip-flops and one-shot circuits

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Read Chapter #7 Flip-Flops and Related Devices with the following modifications:

- Sec. 7-1 Latches: Read all
- Sec. 7-2 Edge-Triggered Flip-Flops: Read all
- Sec. 7-3 Flip-Flop Operating Characteristics: Read all
- Sec. 7-4 Flip-Flop Applications: Read all
- Sec. 7-5 One-Shots: Read all
- Sec. 7-6 The 555 Timer: Read all
- Sec. 7-7 Troubleshooting: Read all
- Sec. 8-8 Programmable Logic: SKIP

Self Test (P. 414): 1 through 10

Homework Problems: (Answers to odd numbered problems are at the back of your text)
 [selected even answers]

- 1, 3, 7
- 12, 13, 14, 15
- 20, 21, 22[C is 32ns and Q is low for first 8ns after rising edge of C]
- 25
- 27
- 30 [28.6Hz]
- 32 [an internally open J input]
- 33, 34

Laboratory 7: Flip-flops Counter with Display

Chapter #8 Counters

Objectives:

- Describe the difference between an asynchronous and a synchronous counter
- Analyze counter timing diagrams
- Analyze counter circuits
- Explain how propagation delays affect the operation of a counter
- Determine the modulus of a counter
- Modify the modulus of a counter
- Recognize the difference between a 4-bit binary counter and a decade counter
- Use IC counters in various applications
- Design a counter that will have any specified sequence of states

Read Chapter #8 Counters with the following modifications:

- Sec. 8-1 Asynchronous Counter Operation: Read all
- Sec. 8-2 Synchronous Counter Operation: Read all
- Sec. 8-3 *through* 8-6: SKIP
- Sec. 8-7 Counter Applications: Read all
- Sec. 8-8 Logic Symbols with Dependency Notation: SKIP

Self Test (P. 481): 1 through 6

Homework Problems: (Answers to odd numbered problems are at the back of your text)
[selected even answers]

1, 2, 3, 4
5, 6,

Laboratory: Final Written and Oral Report

Chapter #9 Shift Registers

Objectives:

- Identify the basic forms of data movement in shift registers
- Explain how serial in/serial out, serial in/parallel out, parallel in/serial out and parallel in/parallel out shift registers operate
- Describe how a bidirectional shift register operates
- Introduce a Johnson counter and ring counter
- Use a shift register as a time-delay device
- Use a shift register to implement a serial-to-parallel data converter

Read Chapter #9 Shift Registers with the following modifications:

- Sec. 9-1 Basic Shift Register Functions: Read all
- Sec. 9-2 Serial In/Serial Out Shift Registers: Read all I
- Sec. 9-3 Serial In/Parallel Out Shift Registers: Read all
- Sec. 9-4 Parallel In/Serial Out Shift Registers: Read all
- Sec. 9-5 Parallel In/Parallel Out Shift Registers: Read all
- Sec. 9-6 Bidirectional Shift Registers: Read all
- Sec 9-7 Shift Register Counters: Read all
- Sec. 9-8 Shift Register Applications: Read all
- Sec. 9-9 Logic Symbol Dependency: SKIP
- Sec. 9-10 Troubleshooting: Read all

Self Test (P. 528): 1 through 10

Homework Problems: (Answers to odd numbered problems are at the back of your text)
[selected even answers]

1, 2
3, 5, 7
9
23

Laboratory: Final Written and Oral Report

Chapter #10 Memory and Storage (Selected readings)

Objectives:

- Define the basic memory characteristics
- Explain what a RAM is and how it works
- Explain the difference between static RAMs (SCRAM) and dynamic RAMs (DRAMS)

Read Chapter #10 Memory and Storage with the following modifications:

- Sec. 10-1 Basics of Semiconductor Memory: Read all
- Sec. 10-2 Random-Access Memories: Read only P. 542 - 547 (top)
- Sec. 10-3 Rom's: Read all
- Sec. 10-4 PROM's and EPROM's: Read all
- Sec. 10-5 Flash: Read all
- Sec 10.6 Memory Expansions: SKIP
- Sec. 10-7 Special Types of Memory: Read all
- Sec. 10-8 Magnetic and Optical Storage: Read all
- Sec. 10-9 Troubleshooting: Read all

Self Test (P. 683): 1 through 8 and 13

Homework Problems: (Answers to odd numbered problems are at the back of your text)
[selected even answers]

1, 2, 3, 4 [$0A_{16} = 0000\ 1010_2 = 10_{10}$, $3F_{16} = 0011\ 1111_2 = 63_{10}$, $CD_{16} = 1100\ 1101_2 = 205_{10}$]

5, 6 [Address: $A_0 - A_8$, Data: $DI_0 - DI_7$, etc], 7

11

15

23

Laboratory: Final Written and Oral Report

Chapter #13 Introduction to Digital Signal Processing (Selected readings)

Objectives:

- List the essential elements in a digital signal processing system
- Explain how analog signals are converted to digital form
- Discuss the purpose of filtering
- Describe the sampling process
- State the purpose of analog-to-digital conversion
- Explain how several ADCs operate
- Explain the basic concepts of a digital signal processor (DSP)
- Name some of the functions that a DSP perform
- State the purpose of digital-to-analog conversion
- Explain how DACs operate

Read Chapter #13 Introduction to Digital Signal Processing with the following modifications:

- Sec. 13-1 Digital Signal Processing Basics: Read all
- Sec. 13-2 Converting Analog Signals to Analog: Read all I
- Sec. 13-3 Analog-to-digital Conversion Methods: Read only P. 774 / 775
- Sec. 13-4 The Digital Signal Processor (DSP): Read only P. 776 - 778 (top)
- Sec. 13-5 Digital-to-Analog Conversion Methods: Read all

Self Test (P. 777): 1 through 8

Homework Problems: (Answers to odd numbered problems are at the back of your text)
[selected even answers]

1, 3

4, 5, 9

10 [200], 11

23, 24 [For each interval: -0.50, -0.75, -2.00, -3.75, -3.50, etc], 25

Laboratory: Final Written and Oral Report

